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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Paper No. 13

Application Number: 09/410,160

Filing Date: September 30, 1999

Appellant(s): BELL ET AL.

Christopher P. Maiorana, Reg. No. 42,829
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/11/03.

(1) *Real Party in Interest*

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A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is substantially correct, all claims 1-20 are rejected. There are two minor errors:

First, the Examiner withdraws all 35 USC 112 rejections. Specifically, the Examiner withdraws all pending enablement rejections (claims 1 and 7) due to Applicant's persuasive

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assertions. Also, the Examiner withdraws all pending indefiniteness rejections (claim 7) due to Applicant's persuasive assertions.

Second, claim 17 does not belong in issue (ii). Specifically, claim 17 does not belong in issue (ii), because claim 17 depends from claim 8 which uses Higgins US Patent 6,397,349 as prior art. The Examiner introduces a new issue (vi) to consider claim 17.

(vi) claim 17 is patentable under 35 USC 103 over Applicant's Admission in view of Kablanian and Higgins and Tzori. Note that claim 17 does not belong in issue (ii), because claim 17 depends from claim 8 which uses Higgins US Patent 6,397,349 as prior art.

Applicant's brief points out that the pending rejection of claim 17 does not explicitly list Higgins. However, Applicant does correctly interpret the rejection of claim 17 as including Higgins. See Applicant's Brief pages 57-64, which note this inconsistency for the first time. The Examiner regrets the inconvenience caused by this minor inconsistency.

Thus, the applicant is correct with respect to all of the issues except 35 USC 112 rejections, and claim 17, as discussed above.

(7) *Grouping of Claims*

Appellant's brief includes a statement that claims of groups 1-10 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

See Brief page 10 for a list of groupings of claims, and see Brief pages 73-75 for detailed reasons.

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,841,967	SAMPLE	11-1998
6,202,044	TZORI	3-2001
6,397,349	HIGGINS	5-2002
5,764,878	KABLANIAN	6-1998

Portions of Applicant's specification Background section are interpreted as Admissions of prior art, due to the use of the term "conventional".

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-20 are rejected under 35 USC 103 as unpatentable. These rejections are set forth in prior Office Action, Paper No. 7, paragraphs 42-125. All 35 USC 103 rejections are maintained. No other rejections are maintained, the 35 USC 112 rejections are withdrawn.

HIGGINS, CLAIM 17. Applicant's brief persuasively points out that the 35 USC 103 rejection of claim 17 omits explicit reference to Higgins, and that said Higgins is used as prior art in the parent claim 8. Applicant correctly interprets the rejection of claim 17 as being in view of Higgins. The rejection of claim 17 below should be interpreted (implicitly) as "further in view of Higgins".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the

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time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

Determining the scope and contents of the prior art.

Ascertaining the differences between the prior art and the claims at issue.

Resolving the level of ordinary skill in the pertinent art.

Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable.

Claim 1 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.

Claim 1 (amended) is an independent claim with 3 limitations.

A-"enumeration of a plurality of fuses" is disclosed by Applicant's Admission at Specification Page 1 line 11 "Conventional methods exist to automate enumeration of all fuse locations on a die". Note that *Constant v. Advanced Micro-Devices*, 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988) states that Applicant's "own admission during prosecution...is binding upon him".

B-"compiling data for each one of said plurality of fuses, wherein said data comprises simulation path data" is admitted by Applicant at Specification Page 1 line 16, "The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation".

Note that MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art." Further, *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Further, *Constant v. Advanced Micro-Devices*, 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988) states that Applicant's "own admission during prosecution...is binding upon him". Applicant's Admissions apparently does not expressly disclose the remaining limitation.

C-“simulating said design with at least one of said fuses programmed for said repair to verify said repair” is disclosed by Kablanian at Column 2 lines 5-11, “External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell”.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5.

Claim 2 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Tzori.

Claim 2 (amended) depends from Claim 1 (amended) with one additional limitation.

Applicant’s Admission does not appear to expressly disclose the additional limitation.

“simulation path data comprises verilog simulation path data” is disclosed by Tzori at Column 1 line 28 “Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules”.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

Claim 3 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.

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Claim 3 (amended) depends from Claim 14 with one additional limitation.

Applicant's Admission does not appear to expressly disclose the additional limitation.

“said schematic path data comprises schematic paths, properties, hierarchy and a verilog path” is disclosed by Tzori at Column 1 line 28 “Performing a Verilog simulation requires that a digital logic designer employ a computer program model for the system by aggregating into a simulation computer program various software modules. The software modules making up a Verilog model include modules for each digital logic circuit included in the simulation, for specifying interconnections among the Verilog logic circuit modules”.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

Claim 4 (twice amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian and Sample.

Claim 4 (twice amended) depends from Claim 1 (amended) with one additional limitation.

Applicant's Admission does not appear to expressly disclose the additional limitation.

“step (B) further comprises the sub-step of: generating a list of layout coordinates and paths as part of said compiling” is disclosed by Sample at FIG 13 element 140 “NETLIST GENERATOR” and element 148 “PART, PLACE, ROUTE”.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Sample to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and “the transistor list or layout specification is used to bum [sic] fuses” according to Sample at Column 1 line 46.

Claim 5 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.

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Claim 5 (amended) depends from Claim 1 (amended) with one additional limitation.

“generating a fuse report” is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”. Merriam-Webster’s Collegiate Dictionary Tenth Edition defines “report” as “to give an account of : RELATE...to describe as being in a specified state”.

Thus, note that each “manual association” is a “fuse report” for a single fuse. Further, even if “report” were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.

Claim 6 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.

Claim 6 (amended) depends from Claim 5 (amended) with one additional limitation.

“listing physical location of one or more devices in response to said fuse reports” is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”. Merriam-Webster’s Collegiate Dictionary Tenth Edition defines “report” as “to give an account of : RELATE...to describe as being in a specified state”. Thus, note that each “manually associate” constitutes a “fuse report” for a single fuse. Further, even if “report” were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.

Claim 7 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.

Claim 7 (amended) depends from Claim 1 (amended) with one new limitation.

“generating a repair file that predicts said at least one of said fuses programmed for said repair” is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods

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exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "file" as "a collection of related data records". Thus, note that each "manual association" is a "file" for a single fuse. Further, even if "file" were interpreted to require a file of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states "It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced".

Claim 8 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian and Higgins.

Claim 8 (amended) depends from Claim 7 (amended) with one additional limitation.

"creating a repair program in response to said repair file" is disclosed by Higgins Column 1 line 20 "Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to "determine the optimal utilization" according to Kablanian at Column 2 line 5, and because "repair procedures result in higher yields" according to Higgins Column 1 line 24.

Claim 9 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian and Higgins.

Claim 9 (amended) depends from Claim 8 (amended) with one additional limitation.

"verifying a function of said design in response to said repair program" is disclosed by Tzori at Column 1 line 17 "Various different software and hardware systems exist for simulating and/or emulating".

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to "determine the optimal utilization"

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according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

Claim 10 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins.

Claim 10 (amended) depends from Claim 8 (amended) with one additional limitation.

“listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses” is disclosed by Applicant’s Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”.

Claim 11 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Higgins and Official Notice.

Claim 11 (amended) depends from Claim 10 (amended) with one new limitation.

“storing said coordinates in a memory” is disclosed by is disclosed by Official Notice that it is well known in the art to store coordinates in memory for future use or to create a permanent record.

Applicant is entitled to traverse the official notice according to MPEP § 2144.03. However, MPEP § 2144.03 further states “See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice).”

Specifically, In re Boon, 169 USPQ 231, 234 states “as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. **We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed**”. Further note that 37 CFR § 1.671(c)(3) states “Judicial notice means official notice”. Thus, a

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traversal by the Applicant that is merely “a bald challenge, with nothing more” will be given very little weight.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins and Official Notice to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24, and to store coordinates in memory for future use or to create a permanent record according to Official Notice.

Claim 12 (amended) is rejected under 35 U.S.C. 103(a).

Claim 12 (amended) is an independent “apparatus” claim with the same limitations as Claim 1, and thus is rejected for the same reasons.

Claim 13 (amended) is rejected under 35 U.S.C. 103(a).

Claim 13 (amended) is an “apparatus” claim with “means for” language and with the same limitations as Claim 1, and thus is rejected for the same reasons.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s

Admission and Kablanian.

Claim 14 depends from Claim 1, with one additional limitation.

“**said data further comprises schematic path data**” is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s

Admission and Kablanian.

Claim 15 depends from Claim 1, with one additional limitation.

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“said data further comprises physical layout data” is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian.

Claim 16 depends from Claim 1, with one additional limitation.

“mapping a plurality of co-ordinates of said fuses to a plurality of verilog statements” is disclosed by Applicant’s Admission at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.”

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant’s Admission and Kablanian and Tzori.

Claim 17 depends from Claim 1, with one additional limitation.

“checking said repair file and said repair program for an error” is disclosed by is disclosed by Tzori at Column 1 line 17 “Various different software and hardware systems exist for simulating and/or emulating”.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Tzori to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” according to Tzori Column 1 line 41.

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Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.

Claim 18 depends from Claim 12, with one additional limitation.

“said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design” is admitted by Applicant at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian.

Claim 19 depends from Claim 12, with one additional limitation.

“said first circuit is further configured to collect data relevant to said fuses that are grouped” is admitted by Applicant at Specification Page 1 line 16, “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission and Kablanian and Official Notice.

Claim 20 depends from Claim 12, with one additional limitation.

“said second circuit is further configured to write a report file” is disclosed by is disclosed by Applicant's Admission at Page 1 line 14 “Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time”. Merriam-Webster's Collegiate Dictionary Tenth Edition defines “report” as “to give an account of : RELATE...to describe as being in a specified state”. Thus, note that each “manually associate” constitutes a “fuse report” for a single fuse. Further, even if “report” were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states “It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced”.

Additionally, writing files is disclosed by Official Notice that it is well known in the art to write files for future use or to create a permanent record.

Applicant is entitled to traverse the official notice according to MPEP § 2144.03. However, MPEP § 2144.03 further states “See also *In re Boon*, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice).” Specifically, *In re Boon*, 169 USPQ 231, 234 states “as we held in *Ahlert*, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more, would be all that was needed”. Further note that 37 CFR § 1.671(c)(3) states “Judicial notice means official notice”. Thus, a traversal by the Applicant that is merely “a bald challenge, with nothing more” will be given very little weight.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Official Notice to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5, and to write files for future use or to create a permanent record according to Official Notice.

(11) *Response to Argument*

FORMAT DETAILS. For clarity, the Examiner uses subheadings that follow the Applicant’s brief as closely as possible. Additional subheadings are used for clarity.

Further, the Examiner uses small type size for long quotations. The key portions of long quotations are generally bolded for emphasis, and the remainder of the long quotations is merely provided for context and may be skimmed or skipped as desired.

Additionally, the Examiner makes liberal use of bold face and underlining, to aid in locating key terms and key points.

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(11.B.1) Brief pages 11-14. **Group 1 (claims 1, 14, 15, and 16)** are not patentable over the Background of the Invention section (Applicant's Admission) in view of Kablanian.

Applicant unpersuasively asserts four reasons why a prima facie case for obviousness rejection has not been established. These four unpersuasive assertions are addressed sequentially below:

- no admissions,
- no motivation,
- conflicting interpretations,
- and does not teach all limitations.

(11.B.1.1) **FIRST REASON—ADMISSIONS**, Brief page 11. Applicant unpersuasively asserts that no admission has been made. Applicant states "No evidence has been provided by the Examiner that any admission has been made by the Appellants" at Examiner's brief page 11.

Note that prior Office action, Paper No. 7 paragraphs 24-27 stated, emphasis added:

Regarding admissions, MPEP § 2129 states "When applicant states that something is prior art, it is taken as being available as prior art against the claims". *In re Nomiya*, 509 F.2d 566, 184 USPQ 607, 611 (CCPA 1975) states "admissions...may be considered "prior art" for any purpose, including use as evidence of obviousness under § 103". *Constant v. Advanced Micro-Devices*, 848 F.2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988), "[Applicant's] own admission during prosecution...is binding upon him". Additionally, U.S. Patent and Trademark Office (USPTO), Formulating and Communicating Rejections Under 35 U.S.C. 1037 (Feb. 13, 1991) states when relying on an admission as evidence of obviousness, moreover, it is unnecessary to cite a corroborating reference to support the admission. Also see 37 C.F.R. § 1.104(c)(3).

Specification page 1 line 10-11 states "**Background of the Invention** **Conventional methods...**" Note that MPEP 608.01(c) states "Background of the Invention...the prior art or other information disclosed known to the applicant". Further, note that "conventional" is defined by Merriam-Webster's Collegiate Dictionary Tenth Edition as "lacking originality or individuality : TRITE... ORDINARY, COMMONPLACE ... convention". And note that "convention" is further defined by "usage or custom... and established technique, practice, or device".

Thus, Applicant is correct that disclosures in the "Background of the Invention" are not necessarily admitted prior art. However, when the word "conventional" is used in the background, this appears to create a rebuttable presumption that prior art is being admitted. If Applicant made an explicit statement that this was not prior art, and gave reasons why it was not prior art, then the Examiner would reconsider this interpretation.

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Here, the Applicant merely traverses that an admission has been made, and does not explicitly deny that it is prior art, and does not give reasons why it is not prior art.

Therefore, in the context of the whole specification, the Examiner maintains that these are admissions of prior art.

Thus, the Examiner asserts that the use of the word “**conventional**” in the Background section of the specification is very strong evidence of an admission of prior art, as discussed in MPEP 2129, and MPEP 608.01(c), and 37 CFR 1.104(c)(3).

(11.B.1.2) SECOND REASON—MOTIVATION, Brief page 11-12. Applicant unpersuasively asserts that there is no clear and particular evidence of motivation. Specifically, Applicant states “In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement” at Brief page 11, referring to MPEP 2142. Evidence of reasonable expectation of success has not been specifically addressed, so some explicit discussion is useful.

The claim 1 motivation states “At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian to modify Applicant’s Admission. One of ordinary skill in the art would have been motivated to do this to “determine the optimal utilization” according to Kablanian at Column 2 line 5.”

Note that the claim 1 Applicant’s Admissions are related to fuses on integrated circuit memories (Specification Page 1 line 11 “Conventional methods exist to automate enumeration of all fuse locations on a die”, and Specification Page 1 line 16 “The conventional methods to manually associate the fuse path to the fuse locations...Conventional verilog simulation paths are derived by manual translation”).

Similarly, Kablanian is also related to fuses on integrated circuit memories. Kablanian at Column 2 lines 5-11 states, "External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell".

Thus, one of ordinary skill in the art would have a high expectation of success when combining Kablanian's software for repairing memory lines with Applicant's Admissions (enumeration and association and simulation paths for memory fuses). Note that Kablanian and Applicant's Admission are directed at precisely the same problem, repairing memory defects by enabling alternate paths. In other words, memory fuses are memory lines that may be open circuited by blowing the fuse. Memory fuses may be open circuited by "blowing", and also may be short circuited by "antifuse" equipment. In fact, it appears that Kablanian is automatically (and implicitly) performing Applicant's Admissions.

Note that memory chips generally contain extra (redundant) lines and extra (redundant) sections of memory. If a memory line is defective, then that line may be isolated by "blowing" fuses and alternate paths may be enabled by "unblowing" fuses.

Similarly, if a section of memory is defective, then that defective section may be isolated by blowing fuses, and the memory duties may be routed to another section of memory by enabling alternate memory lines. Thus, Kablanian is addressing precisely the same problems as Applicant's Admissions, although using slightly different terminology.

Additionally, one of ordinary skill in the art would be motivated to use Kablanian's software in order to "determine the optimal utilization" according to Kablanian at Column 2 line 5. Criteria for determining the optimal utilization may include: simultaneously repairing

multiple failures, minimizing the number of lines which must be altered to create a repair, minimizing capacitance, and so forth.

Optimization is defined as “[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization.” by McGraw–Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1329, 1989.

Thus, there is substantial motivation, as well as high expectation of success. Further, it appears that Kablanian may implicitly disclose (and automatically perform) all the limitations that are disclosed by Applicant’s Admissions (enumeration and association and simulation paths for memory fuses).

(11.B.1.3) THIRD REASON—MULTIPLE INTERPRETATIONS, Brief page 14. Applicant unpersuasively asserts “The same two sentences [of the specification Background] cannot teach or suggest three different types of data simultaneously” at Brief page 14. This statement lacks any logical analysis supporting the statement. Logically, a single sentence can teach many types of data simultaneously.

Applicant refers to the specification page 1 lines 16-20 (Applicant’s Admissions), which state “The conventional methods to manually associate the fuse path to the fuse locations, or vise [sic] versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog [sic] simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist”.

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The Applicant unpersuasively asserts that this admission cannot simultaneously teach “simulation path data”, and “schematic path data” and “physical layout data”.

Specifically:

“simulation path data” is disclosed by the specification term “simulation path”, and

“schematic path data” is disclosed by the specification term “schematic path”, and

“physical layout data” is disclosed by the terms “fuse path” and “fuse locations” and “netlist”.

Thus, at least three different types of data (closely related data) are taught by the Applicant’s Admissions in the specification. Again, it also appears that these types of data may be inherent in Kablanian.

(11.B.1.4) **FOURTH REASON—ALL LIMITATIONS ARE DISCLOSED, Brief page 12-13. Note that this appears to be the Applicant’s strongest argument regarding any 35 USC 103 rejection, but it is not persuasive.**

Applicant unpersuasively asserts the claim 1 limitation **“simulating said design with at least one of said fuses programmed for said repair to verify said repair”** is not disclosed by Kablanian at Column 2 lines 5-11, “External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell”.

The Examiner admits that the Kablanian terminology does not exactly match the claim terminology, and thus requires further discussion. Therefore, this is the Applicant’s strongest argument.

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Specifically, the Applicant asserts that claim 1 **“simulating”** is not disclosed, and that **“to verify said repair”** is not disclosed. Applicant addresses these terms separately.

SIMULATING. Kablanian’s Column 2 lines 5-11 term **“External software... optimal utilization... repair defective memory lines”** must be interpreted in the view of one of ordinary skill in the art. One of ordinary skill in the art of simulation would be familiar with Tzori column 1 line 23 “Software digital logic system simulators, such as Verilog [language based simulators], are routinely used for designing systems as physically small as individual integrated circuits”. Thus, Tzori’s “Software digital logic simulators” are the type of “External software” disclosed by Kablanian. Note that Tzori has been cited with respect to claims 2 and 17.

Additionally, one of ordinary skill in the art would be familiar with terms of art such as:

“simulate [ENG] To mimic some or all of the behavior of one system with a different, dissimilar system, particularly with computers, models, or other equipment”, according to McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1737, 1989; and

“Simulation is the imitation of the operation of a real-world process or system over time. Simulation involves the generation of an artificial history of the system and the observation of that artificial history to draw inferences concerning the operating characteristics of the real system that is represented. Simulation is an indispensable problem-solving methodology for the solution of many real-world problems. Simulation is used to describe and analyze the behavior of a system, ask what-if questions about the real system, and aid in the design of real systems. Both existing and conceptual systems can be modeled with simulation.” according to the Handbook of Simulation, by Jerry Banks, page 3-4, 1998. Note that the Handbook of Simulation specifically addresses modeling existing systems (such as a defective memory) and asking “what-if questions” (such as what-if a given line is repaired).

Thus, one of ordinary skill in the art would interpret Kablanian’s “External software... optimal utilization... repair defective memory lines” as disclosing the claim 1 limitation

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“simulating said design with at least one of said fuses programmed for said repair to verify said repair”. Note that Kablanian’s term “optimal” implies maximizing (or minimizing) some objective function, and thus determines the optimum solution (repair) from a universe of possible repairs. Thus, Kablanian not only discloses “verify said repair”, but even goes one step further in that it selects an optimal repair from a set of possible repairs.

TO VERIFY. Additionally, note that Applicant asserts at Brief page 13 that “In contrast, the claim provides **verifying** the repair **after** simulating the repair.” Emphasis in original.

However, note the exact wording of claim 1: “**simulating** said design with at least one of said fuses programmed for said repair **to verify said repair**”. Emphasis added. The claim 1 limitation uses simulation as a method to “verify” the repair, it does not perform the verification after the simulation, as the Applicant unpersuasively asserts. In summary, claim 1 is interpreted as verifying by simulating, and not interpreted as verifying after simulating.

Additionally, “verifying” by simulating in claim 1 is interpreted as disclosed by Kablanian’s “optimal utilization”. Note that if the simulation of the proposed (or “programmed”) repair of a fuse fails, then the proposed repair can not be optimal. If the simulation of the proposed repair succeeds, then the proposed repair might be the optimal repair.

Optimization is defined as “[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, **effective, or functional** as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization.” by McGraw–Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1329, 1989. Emphasis added.

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Note that the definition of optimization includes “effective, or functional”, and thus discloses the claim 1 term “verify”.

APPLICANT’S INTERPRETATION, FOR DISCUSSION. Hypothetically, for purposes of discussion, if claim 1 is interpreted as verifying after simulation (as the Applicant unpersuasively asserts), then verification after simulation would be disclosed by Kablanian column 2 line 11 “The final process involves retesting the chip using the ATE to ensure that the chip functions properly after being repaired”. It is possible that the Applicant intended physical verification after simulation (per Kablanian’s “final process”), but that is not the plain meaning of the claim as written. The Examiner interprets the claims as written in light of the specification.

As previously stated, this appears to be the Applicant’s strongest argument regarding any 35 USC 103 rejection, and it is not persuasive.

SUMMARY. In summary, the Applicant has made four independent arguments regarding the 35 USC 103 rejections of Group 1 claims 1, 14, 15, and 16. None of these four independent arguments (no admissions, no motivation, conflicting interpretations, and does not teach all limitations) is persuasive.

The rejections of Group 1 are maintained.

(11.2) MAINTAIN REJECTIONS, Brief pages 15-20. **Group 2 (claims 12 and 20)** are not patentable over the Background of the Invention section (Applicant’s Admissions) in view of Kablanian.

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Similar to Applicant's assertions in Group 1 above, the Applicant unpersuasively asserts four reasons why a prima facie case for obviousness rejection has not been established: no admissions, no motivation, conflicting interpretations, and does not teach all limitations.

The Group 2 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, plus one additional reason:

Claim 12 is an "apparatus" claim with the same limitations as claim 1. Applicant persuasively asserts "External software [per Kablanian] is not a circuit per claim 12." Specifically, claim 12 states "a second circuit configured to... perform a simulation".

However, it is well known in the art that instructions can be stored in the form of lines in a memory (software), or instructions can be "hardwired" in a circuit. Software has the advantage of being easily modified, but "hardwire" has the advantage of operating at much higher speeds. The dual nature and relative advantages of software and hardware ("hardwired") are well known in the art. Thus, disclosing processes in software inherently discloses the possibility of performing the same processes using hardware.

Note that Sample Abstract states "Reconfigurable hardware... aid the simulation, and to reduce processing time". Thus, Sample uses a combination of software and hardware to perform the simulation.

(11.3) Brief pages 21-26. **Group 3 (claim 13)** is not patentable over the Background of the Invention section (Applicant's Admissions) in view of Kablanian.

The Group 3 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, as discussed above.

(11.4) Brief pages 26-32. **Group 6 (claims 5 and 6)** are not patentable over the Background of the Invention section (Applicant's Admissions) in view of Kablanian.

The Group 6 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, as discussed above, plus one additional reason.

Applicant unpersuasively asserts, Brief page 31, that one sentence in the specification Background (Applicant's Admissions) cannot disclose multiple limitations. Specifically, Applicant asserts that "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time" at Specification page 1 lines 14-15 cannot simultaneously disclose four different steps: **"generating a fuse report"**, and **"listing physical locations"**, and **"generating a repair file"**, and **"listing an output of a repair program"**.

As previously discussed above in the Group 1 discussion, a single sentence can clearly teach more than one limitation. Therefore Applicant's logical argument fails. A single sentence can teach more than one limitation, and this single sentence does teach all four steps, in the view of one of ordinary skill in the art and in the context of the specification and in the context of the prior art. For convenience, the Examiner presents (below) the relevant paragraphs from the prior Office Action, paper No. 7, with emphasis slightly altered for clarity.

Regarding claim 5, **"generating a fuse report"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "report" as "to give an account of : RELATE...to describe as being in a specified state". Thus, note that each "manual association" is a "fuse report" for a single fuse. Further, even if "report" were interpreted to require a report of multiple fuses, then this would be

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mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states "It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced".

Regarding claim 6, **"listing physical location of one or more devices in response to said fuse reports"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "report" as "to give an account of : RELATE...to describe as being in a specified state". Thus, note that each "manually associate" constitutes a "fuse report" for a single fuse. Further, even if "report" were interpreted to require a report of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states "It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced".

Regarding claim 7, **"generating a repair file that predicts said at least one of said fuses programmed for said repair"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time". Merriam-Webster's Collegiate Dictionary Tenth Edition defines "file" as "a collection of related data records". Thus, note that each "manual association" is a "file" for a single fuse. Further, even if "file" were interpreted to require a file of multiple fuses, then this would be mere duplication of parts according to MPEP 2144.04(VI)(B). Additionally, In re Harza, 274 F.2d 669, 124 USPQ 378, 380 (CCPA 1960) states "It is well settled that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced".

Regarding claim 10, **"listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses"** is disclosed by Applicant's Admission at Page 1 line 14 "Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time".

Note that these claims must be interpreted in view of the other prior art used in the 35 USC 103 rejections, and particularly in view of the rejections of the parent claims. For example,

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regarding claim 10, “listing an output of said repair program must as a list of coordinates” must be interpreted in view of its parent claim 8. In the claim 8 rejection, Higgins Column 1 line 20 states **“Location information is then supplied to a controller for a laser repair device, which achieves a hardware fix.”** In turn, claim 8 depends from claim 7, which depends from independent claim 1.

In the independent claim 1 rejection, the limitation “simulating said design with at least one of said fuses programmed for said repair to verify said repair” is disclosed by Kablanian at Column 2 lines 5-11, **“External software is used to determine the optimal utilization of the redundant memory lines to repair defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip of selective removal through convention laser beam techniques to repair a defective memory cell”.**

When interpreted in the context of Higgins and Kablanian, then Applicant’s Admission discloses all four steps. Additionally, it appears that Higgins and Kablanian themselves strongly imply all four steps as part of their processes, although Higgins and Kablanian do not explicitly state these four steps. Note that Higgins and Kablanian apparently automate the conventional process discussed in Applicant’s Background.

(11.5) MAINTAIN REJECTIONS, Brief pages 32-38. **Group 7 (claim 7)** is not patentable over the Background of the Invention section (Applicant’s Admissions) in view of Kablanian.

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The Group 7 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, and the reasons that the Group 6 assertions were not persuasive, as discussed above.

(11.6) MAINTAIN REJECTIONS, Brief pages 38-44. **Group 10 (claims 18-19)** is not patentable over the Background of the Invention section (Applicant's Admissions) in view of Kablanian.

The Group 10 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, as discussed above.

(11.7) Brief pages 44-50. **Group 4 (claims 2 and 3)** is not patentable over the Background of the Invention section (Applicant's Admissions) in view of Kablanian and Tzori.

Applicant correctly interprets that claim 3 is rejected over the Background (Applicant's Admissions) in view of Kablanian and Tzori. Tzori was inadvertently omitted from the title of the rejection of Claim 3, however Tzori was explicitly cited as prior art and explicitly discussed in the motivation.

The Group 4 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, and one additional reason.

Note that Tzori provides excellent motivation for simulating repairs before performing the repairs, stating "in almost all instances IC [integrated circuit] manufacturers simulate their designs before fabricating even a prototype". Repairing a memory integrated circuit consists of

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isolating damaged sections (and/or lines) and accessing undamaged sections (and/or lines), thus effectively designing a new integrated circuit.

Simulations are relatively inexpensive and fast methods of analyzing new designs, and thus one of ordinary skill in the art would be motivated to simulate a memory repair before performing the repair for the same reasons that a manufacturer would simulate a design before fabricating “even a prototype”. Note that a prototype is a single chip with a unique design, and a repaired chip is also a single chip with a unique (after repair) design.

(11.8) MAINTAIN REJECTIONS, Brief pages 50-57. **Group 5 (claim 4)** is not patentable over the Background of the Invention section (Applicant’s Admissions) in view of Kablanian and Sample.

The Group 5 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, and one additional reason.

Applicant asserts that Sample teaches burning fuses in an actual device, and that there is not adequate motivation to combine with the other prior art. Note that Sample explicitly discloses what is strongly implied in the other prior art. Specifically, Sample provides some detail regarding the repair process disclosed by Kablanian’s “third process”. See Kablanian column 2 line 4 “The next process is one of analysis. External software is used to determine optimal utilization of the redundant memory lines to repair defective memory lines. **The third process is the repair process.** Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through a conventional laser beam techniques to repair a defective memory cell.” Emphasis added.

The analysis results information (optimal design) must somehow be transferred to the laser beam in some useful format. The useful format for the laser beam must contain the exact

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physical location of any target areas, and this exact location may be expressed in Samples FIG 13 element 140 "NETLIST GENERATOR" and element 148 "PART, PLACE, ROUTE".

Thus, Sample merely explains the mechanism or format for transferring information to the laser beam during the repair process of Kablanian. Sample states "the transistor list or layout specification is used to bum [sic] fuses" at Column 1 line 46.

Note that Sample is directed to "reconfigurable hardware such as field programmable gate arrays" at Abstract, and that "reconfiguring" field programmable gate arrays uses precisely the same technology (fuse, and antifuse) as repairing memory integrated circuits. In summary, repairing memory is one specific type of hardware reconfiguration, and field programmable gate arrays are another specific type of hardware configuration.

(11.9) MAINTAIN REJECTIONS, Brief pages 57-64. **Group 8 (claim 8, 10, and 11)** is not patentable over the Background of the Invention section (Applicant's Admissions) in view of Kablanian and Higgins.

The Group 8 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, and the same reasons that the Group 6 assertions were not persuasive, and one additional reason.

Regarding motivation, the Applicant unpersuasively states "the asserted motivation that "repair procedures result in higher yields" is a conclusory statement.", at Brief page 50.

Applicant is referring to the motivation for the claim 8 rejection, which states, "At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to

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“determine the optimal utilization” according to Kablanian at Column 2 line 5, and because “repair procedures result in higher yields” according to Higgins Column 1 line 24.”

Higgins is used as prior art because it explicitly discloses what is merely implied (and probably inherent) in the other prior art. Specifically, Higgins explicitly discloses that location information must be supplied to the laser repair device in order to achieve a hardware fix. Additionally, Higgins gives clear and explicit motivation for repairing defective chips, specifically because “repair procedures result in higher yields” at column 1 line 24. Transferring the location information to the laser repair device is an essential part of achieving the hardware fix, and the additional limitation of claim 8 is motivated by “higher yields”.

Thus, Applicant’s Group 8 assertions are not persuasive.

(11.10) **MAINTAIN REJECTIONS**, Brief pages 57-64. **Group 9 (claims 9 and 17)** is not patentable over the Background of the Invention section (Applicant’s Admissions) in view of Kablanian and Higgins and Tzori.

Applicant correctly points out that the claim 17 rejection does not explicitly include the Higgins reference, but that claim 17 depends from claim 8 which uses Higgins. Thus, Applicant correctly interprets the claim 17 rejection as being rejected over the Background of the Invention section (Applicant’s Admissions) in view of Kablanian and Higgins and Tzori. The Examiner regrets any inconvenience caused by this minor error.

The Group 9 assertions are not persuasive for the same reasons that the Group 1 assertions were not persuasive, and the same reasons that the Group 6 assertions were not persuasive, and one additional reason.

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Applicant unpersuasively asserts, at Brief page 68, that the motivation of claim 9 from Tzori is a conclusory statement. In full, the claim 9 motivational statement is: "At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Kablanian and Higgins to modify Applicant's Admission. One of ordinary skill in the art would have been motivated to do this to "determine the optimal utilization" according to Kablanian at Column 2 line 5, and because "repair procedures result in higher yields" according to Higgins Column 1 line 24, and because **"Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype"** according to Tzori Column 1 line 41." Emphasis added.

The point is that it is standard procedure ("in almost all instances") to simulate IC designs before fabrication, and that the same standard procedure (and the same motivation for the standard procedure) applies to simulating repairs of memory integrated circuits before performing the actual repairs.

Thus, the Group 9 assertions are not persuasive.

(11.11) GROUPS 1-10 ARE SEPARATELY PATENTABLE. Brief pages 73-75.

Applicant gives detailed reasons why each of Groups 1-10 are separately patentable. The Examiner agrees with these reasons.

(11.12) SUMMARY.

All pending 35 USC 112 rejections are withdrawn (claims 1 and 7).

All pending 35 USC 103 rejections are maintained (claims 1-20).

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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